

Docket: GS 149

METHOD OF FORMING NARROW TRENCHES IN SEMICONDUCTOR SUBSTRATES

FIELD OF THE INVENTION

[0001] This invention relates to methods of forming narrow trenches in semiconductor substrates.

BACKGROUND OF THE INVENTION

[0002] Narrow trenches are commonly desired during fabrication of a wide array of semiconductor devices. Hence, although a specific example concerning the utility of narrow trenches is discussed below in connection with trench MOSFET devices, it is noted that narrow trenches have utility throughout the semiconductor field.

[0003] A trench MOSFET (metal-oxide-semiconductor field-effect transistor) is a transistor in which the channel is formed vertically and the gate is formed in a trench extending between the source and drain. The trench, which is lined with a thin insulator layer such as an oxide layer and filled with a conductor such as polysilicon (i.e., polycrystalline silicon), allows less constricted current flow and thereby provides lower values of specific on-resistance. Examples of trench MOSFET transistors are disclosed, for example, in U.S. Patent Nos. 5,072,266, 5,541,425, and 5,866,931, the disclosures of which are hereby incorporated by reference.

[0004] As a specific example, Figure 1 illustrates half of a hexagonally shaped trench MOSFET structure 21 disclosed in U.S. Patent No. 5,072,266. The structure includes an n+ substrate 23, upon which is grown a lightly doped n epitaxial layer 25 of a predetermined depth d_{epi} . Within the epitaxial layer 25, p body region 27 (p, p+) is provided. In the design shown, the p body region 27 is substantially planar (except in a central region) and typically lays a distance d_{min} below the top surface of the epitaxial layer. Another layer 28 (n+) overlying most of the p body region 27 serves as source for the device. A series of hexagonally shaped trenches 29 are provided in the epitaxial layer, opening toward the top and having a predetermined depth d_{tr} . The trenches 29 are typically lined with oxide and filled with conductive polysilicon, forming the gate for the

Docket: GS 149

MOSFET device. The trenches 29 define cell regions 31 that are also hexagonally shaped in horizontal cross-section. Within the cell region 31, the p body region 27 rises to the top surface of the epitaxial layer and forms an exposed pattern 33 in a horizontal cross section at the top surface of the cell region 31. In the specific design illustrated, the p+ central portion of the p body region 27 extends to a depth d_{\max} below the surface of the epitaxial layer that is greater than the trench depth d_{tr} for the transistor cell so that breakdown voltage is away from the trench surface and into the bulk of the semiconductor material.

[0005] A typical MOSFET device includes numerous individual MOSFET cells that are fabricated in parallel within a single chip (i.e., a section of a semiconductor wafer). Hence, the chip shown in Fig. 1 contains numerous hexagonal-shaped cells 31 (portions of five of these cells are illustrated). Cell configurations other than hexagonal configurations are commonly used, including square-shaped configurations. In a design like that shown in Fig. 1, the substrate region 23 acts as a common drain contact for all of the individual MOSFET cells 31. Although not illustrated, all the sources for the MOSFET cells 31 are typically shorted together via a metal source contact that is disposed on top of the n+ source regions 28. An insulating region, such as borophosphosilicate glass (not shown) is typically placed between the polysilicon in the trenches 29 and the metal source contact to prevent the gate regions from being shorted with the source regions. Consequently, to make gate contact, the polysilicon within the trenches 29 is typically extended into a termination region beyond the MOSFET cells 31, where a metal gate contact is provided on the polysilicon. Since the polysilicon gate regions are interconnected with one another via the trenches, this arrangement provides a single gate contact for all the gate regions of the device. As a result of this scheme, even though the chip contains a matrix of individual transistor cells 31, these cells 31 behave as a single large transistor.

[0006] Demand persists for trench MOSFET devices having ever-lower on-resistance. One way to reduce on-resistance is to increase cell density. Unfortunately, the gate charges associated with trench MOSFET devices also increase when cell density is increased. As a result, steps need to be taken to reduce such gate charges. As noted in JP05335582, the oxide film at the trench sidewall of a trench MOSFET device forms the channel within the P-body region. The oxide film at the bottom of the trench, on the

Docket: GS 149

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] Fig. 1 is a schematic cross-sectional view of a trench MOSFET device in the prior art.

[0019] Figs. 2A through 2D are schematic cross-sectional views illustrating a process for forming a narrow trench, according to an embodiment of the present invention.

[0020] Figs. 3A and 3B are schematic cross-sectional views illustrating a method of increasing sidewall spacer width, according to an embodiment of the present invention.

[0021] Figs. 4A through 4C are schematic cross-sectional views illustrating a method of making a trench MOSFET device, according to an embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION

[0022] The present invention now will be described more fully hereinafter with frequent reference to the accompanying drawings, in which preferred embodiments of the present invention are shown. This invention may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein.

[0023] According to an embodiment of the present invention, a semiconductor substrate is the preferred substrate. The semiconductor substrate can be any such substrate known in the art, including elemental semiconductor substrates, such as silicon or germanium, or compound semiconductor substrates, such as GaAs, AlAs, GaP, InP, GaAlAs, and so forth. The semiconductor substrate can be single crystal, polycrystalline and/or amorphous, and it can be doped or undoped. A specific example of a semiconductor substrate is presented in connection with Figs. 2A through 2D. Referring to Fig. 2A, a silicon semiconductor substrate 201 is shown, which consists of an N⁺ doped silicon wafer 200 having an N doped silicon epitaxial layer 202 disposed thereon.

[0024] Once the substrate is selected, a first layer of a masking material that is appropriate for forming a trench mask is provided on the substrate and patterned using any appropriate technique known in the art. For example, a first masking material layer

6

Docket: GS 149

epitaxial layer 202 is anisotropically etched, for example by reactive ion etching, through the final apertures 205f in the two-component oxide mask (which includes both the patterned first mask oxide layer 203 and the sidewall spacers 203s), resulting in trenches 207 as shown in Fig. 2D. The widths of the trenches 207 reflect the final apertures 205f, rather than the initial apertures 205i.

[0031] As noted above, narrow trench widths are useful in connection with trench MOSFET devices in that the gate-drain charges associated with such devices are reduced, among other effects. A method of forming a typical trench MOSFET device that incorporates the two-component trench mask of the present invention is briefly discussed here in connection with Figs. 4A-4C.

[0032] Turning now to Fig. 4A, an N doped epitaxial layer 202 is initially grown on an N+ doped substrate 200. A P-type region 204 is then formed in upper portion of the epitaxial layer 202 by implantation and diffusion. Subsequently, a two-component trench mask including both a patterned mask oxide layer 203 and oxide sidewall spacer portions 203s is formed as discussed above in connection with Figs. 2A-2C. The resulting structure is shown in Fig. 4A.

[0033] Trenches are then etched as discussed in connection with Fig. 2D above. Discrete P-type regions 204 are established as a result of this trench-forming step. The two-component trench mask is then removed and an oxide layer 210 is grown over the surface of the device, typically by dry oxidation at elevated temperature. Portions of the oxide layer 210 ultimately form the gate oxide regions for the finished device. The surface of the structure is then covered, and the trenches are filled, with a polysilicon layer, typically using CVD. The polysilicon is typically doped N-type to reduce its resistivity. The polysilicon layer is then etched, forming polysilicon gate regions 211. The resulting structure is shown in Fig. 4B.

[0034] Subsequently, n+ source regions 212 are formed in upper portions of the epitaxial layer via an implantation and diffusion process. BPSG (borophosphosilicate glass) regions 216 are then formed, typically by deposition, masking and etching processes, covering polysilicon regions 211 and a portion of the oxide regions 210. Finally, a metal contact layer (e.g., aluminum) is deposited, forming source contact 218.

Docket: GS 149

The resulting structure is shown in Fig. 4C. A separate metal gate contact is also typically connected to a gate runner portion of the polysilicon that is located outside of the cell region of the trench MOSFET (not shown). Furthermore, a metal drain contact is also typically provided in connection with the semiconductor substrate (not shown).

[0035] Although various embodiments are specifically illustrated and described herein, it will be appreciated that modifications and variations of the present invention are covered by the above teachings and are within the purview of the appended claims without departing from the spirit and intended scope of the invention.